Virtual Qualification of Electronic Hardware

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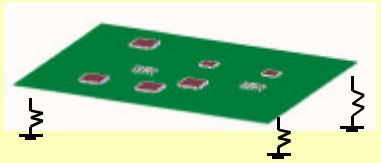
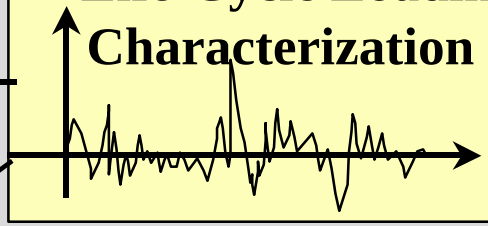
Virtual Qualification Methodology

Design Capture



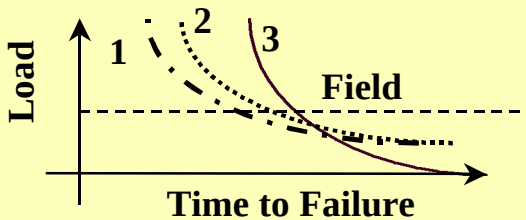
Load Transformation

Life-Cycle Loading Characterization



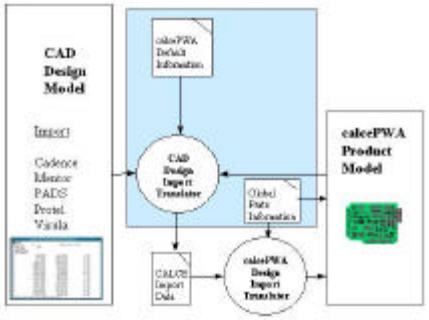
Failure Risk Assessment

Ranking of Potential Failures Under Life-Cycle Loads



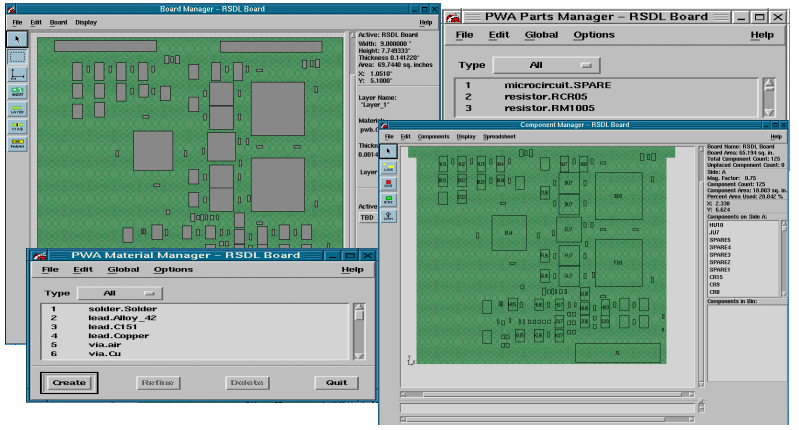
Physical Verification: Test Setup, Specimen Characterization, Accelerated Stress Test

Virtual Qualification Infrastructure for Circuit Card Assemblies (CCAs) : calcePWA 3.1

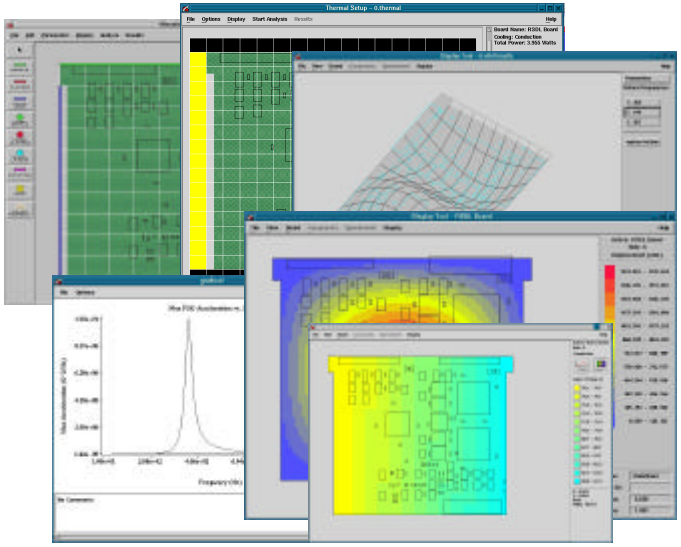


Computer Design Data

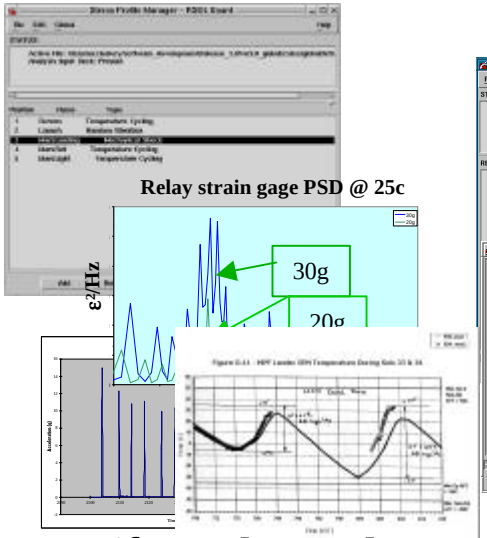
Toolbox



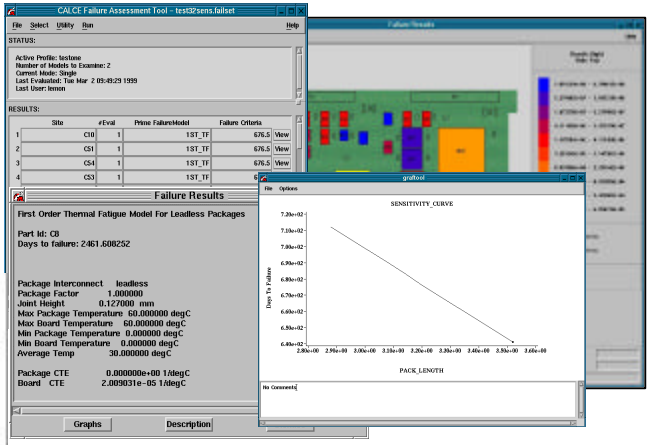
Product Modeling and Databases



Load Transformation



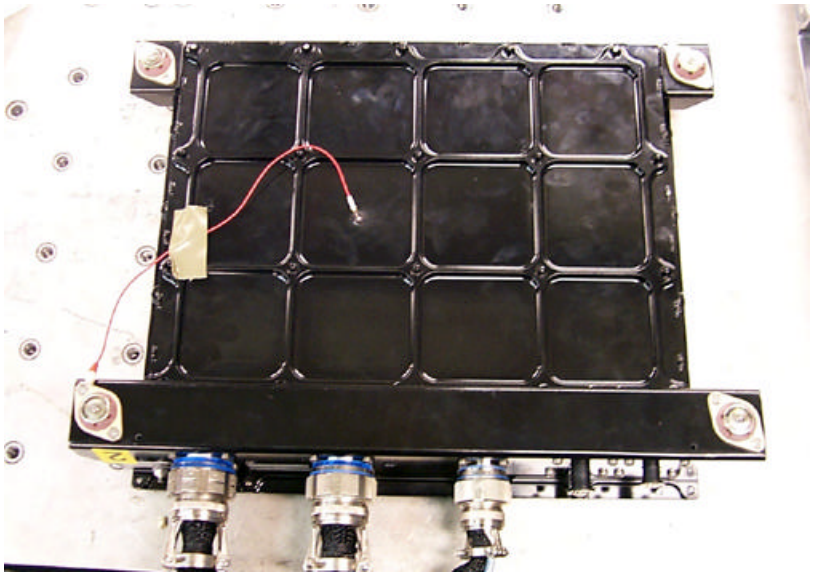
Life Cycle Load Characterization



Failure Risk Assessment & sensitivity analysis

Avionics Application Demonstration

AS900 Engine Family



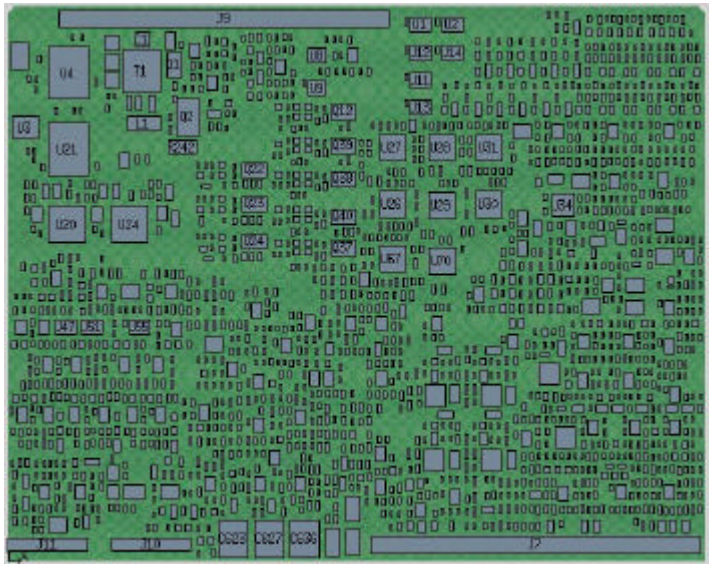
Electronic Chassis

Electronic hardware is to be mounted on engine and operate reliably under high temperature and vibration loading conditions. To achieve an adequate design, reliability was considered upfront in the design process and simulation techniques were applied to virtually qualify the assembly.

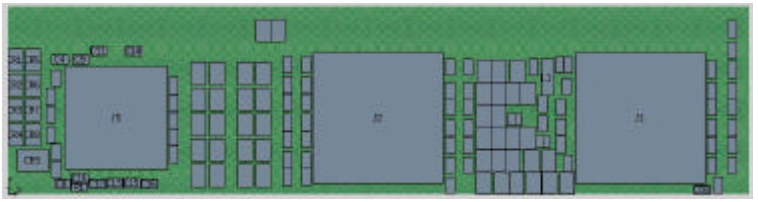
Steps Involved in calcePWA
Virtual Qualification Assessment of CCAs

- Collect design information
- Develop design model
- Transform environment and operation loads
    - Perform thermal analysis
    - Perform vibration analysis
- Perform failure assessment
- Review and verify results
- Refine model (if necessary)

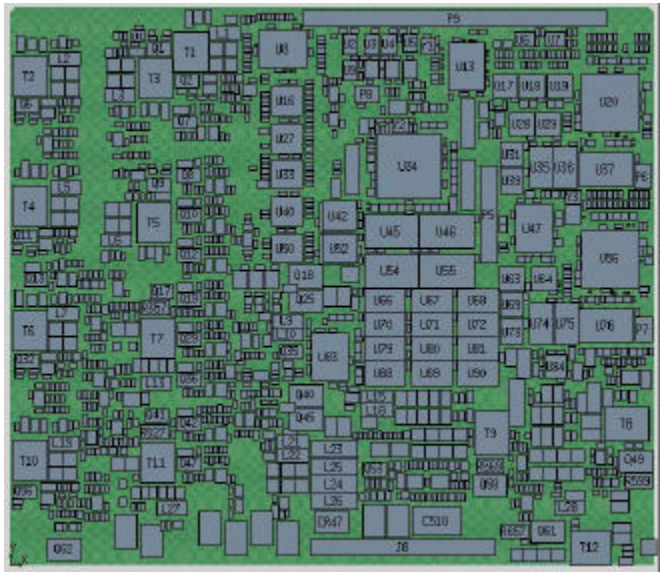
Design Capture
AS900 Circuit Card Assemblies



I/O
212 Parts
2122 Components
10 Layer FR4
Copper Metallization

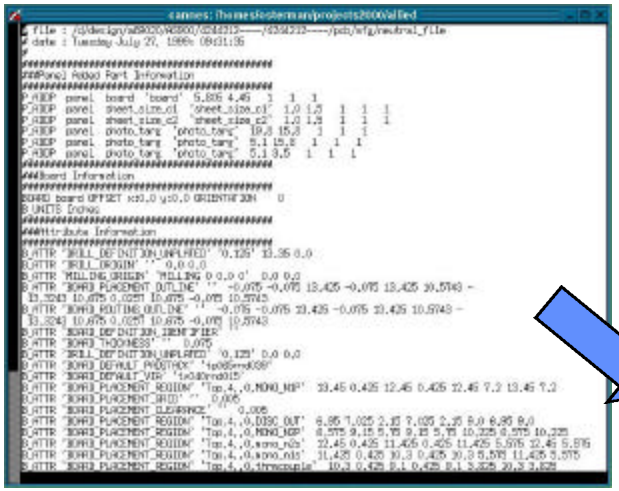


EMI
16 Parts
328 Components
10 Layer FR4
Copper Metallization

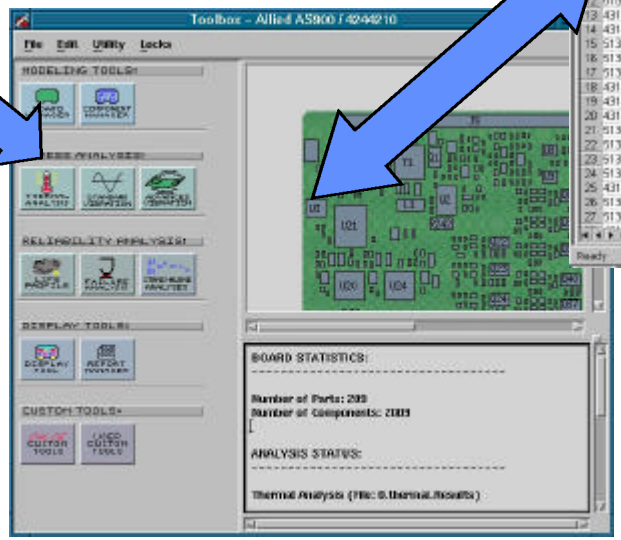


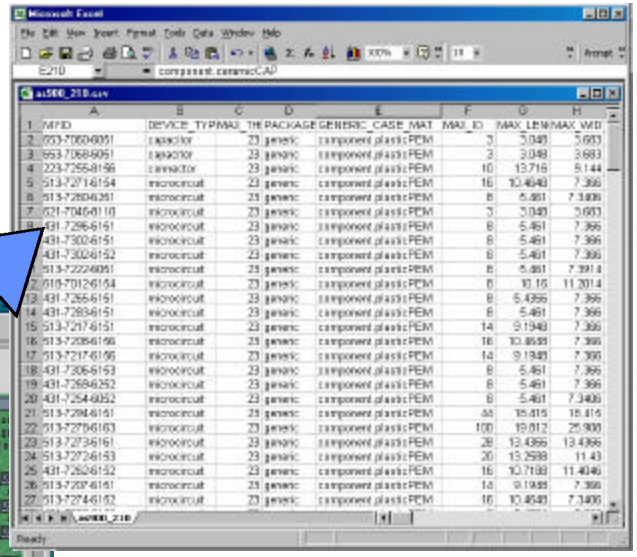
CPU
167 Parts
1622 Components
10 Layer FR4
Copper Metallization

Design Capture and Model Development



Mentor Neutral Files

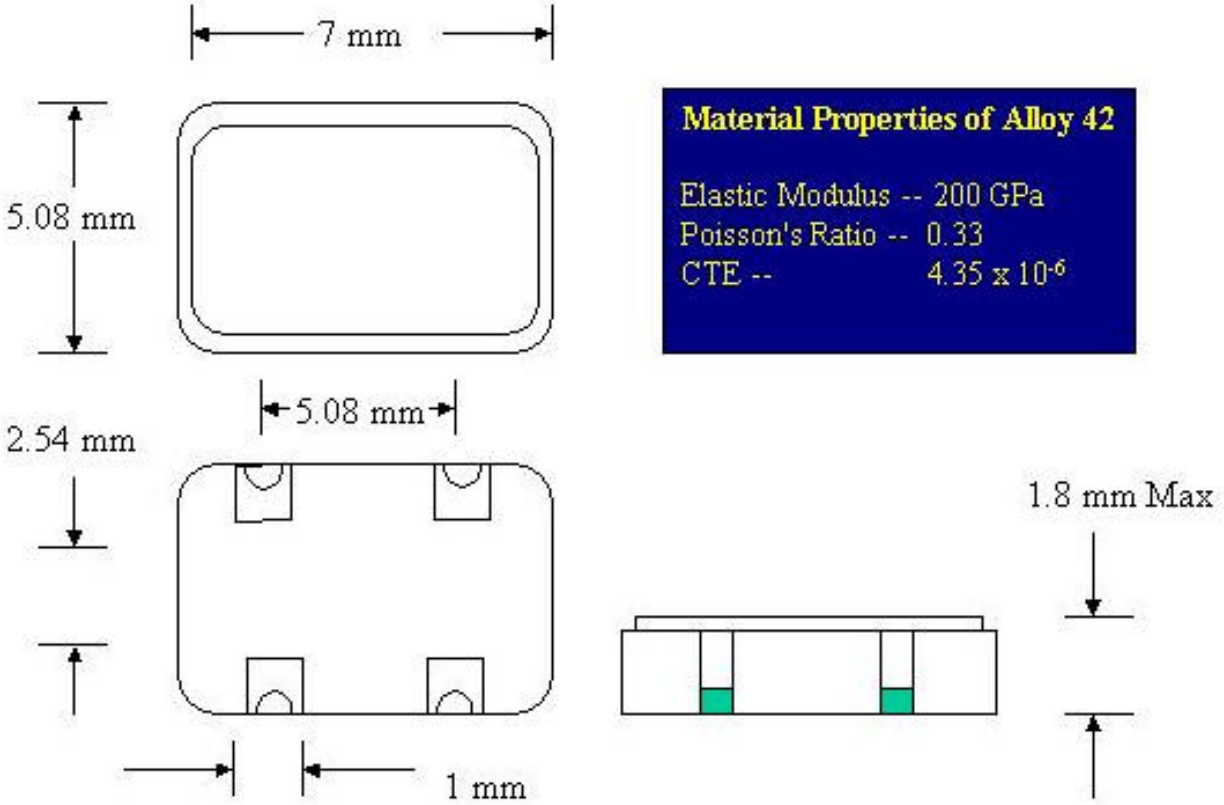




MS Excel Data

Design information was capture using import facility in calcePWA. Subsequent data processing of part information was done in spreadsheets and within software. Material data from calcePWA library was used in modeling board and component structures.

Design Capture: Part Models



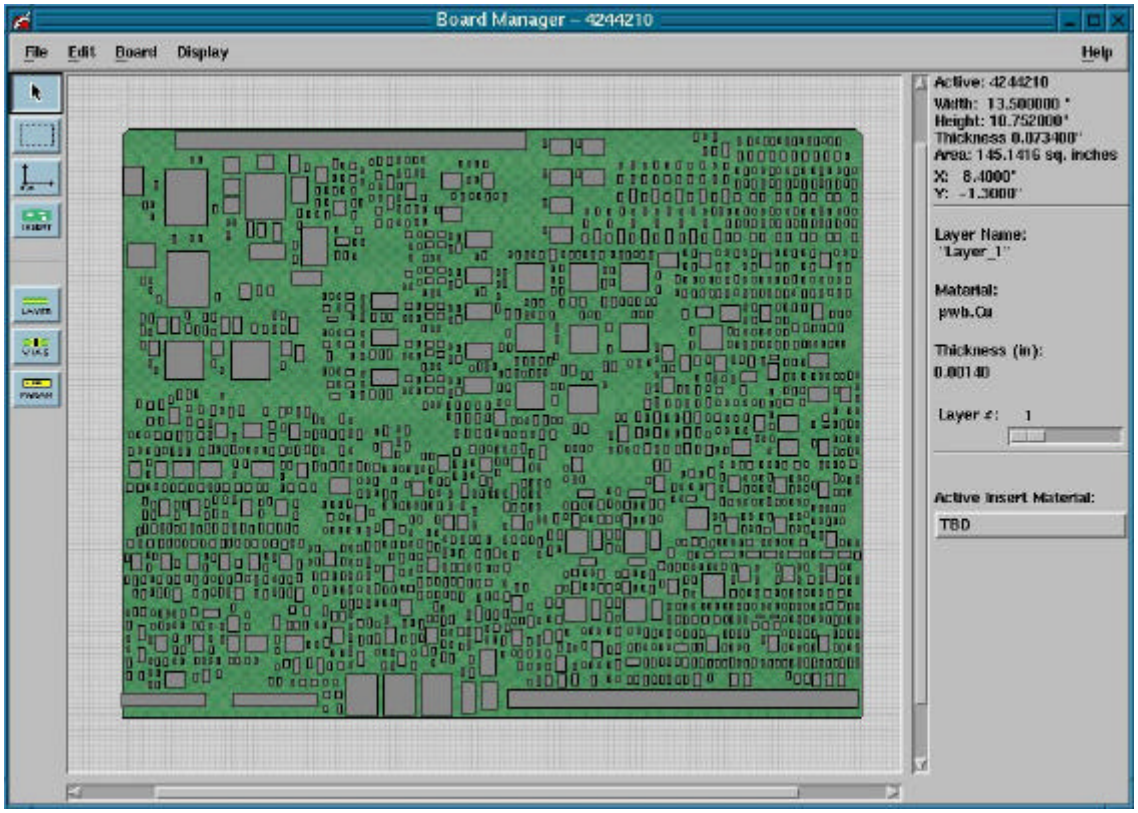
Package
- Effective Material
- Attach Positions

Interconnect
- Pad Size
- Lead Geometry

Attach
- Joint Height
- Pad Size

Operational
- Power dissipation

Design Capture: Board Model



- Board
  - Layered Structure
    - Signal
    - Dielectric
  - Regions of
    - Inserts
- Vias
  - Drill Size
  - Plating Thickness
  - Pad Diameter
  - Plating Material

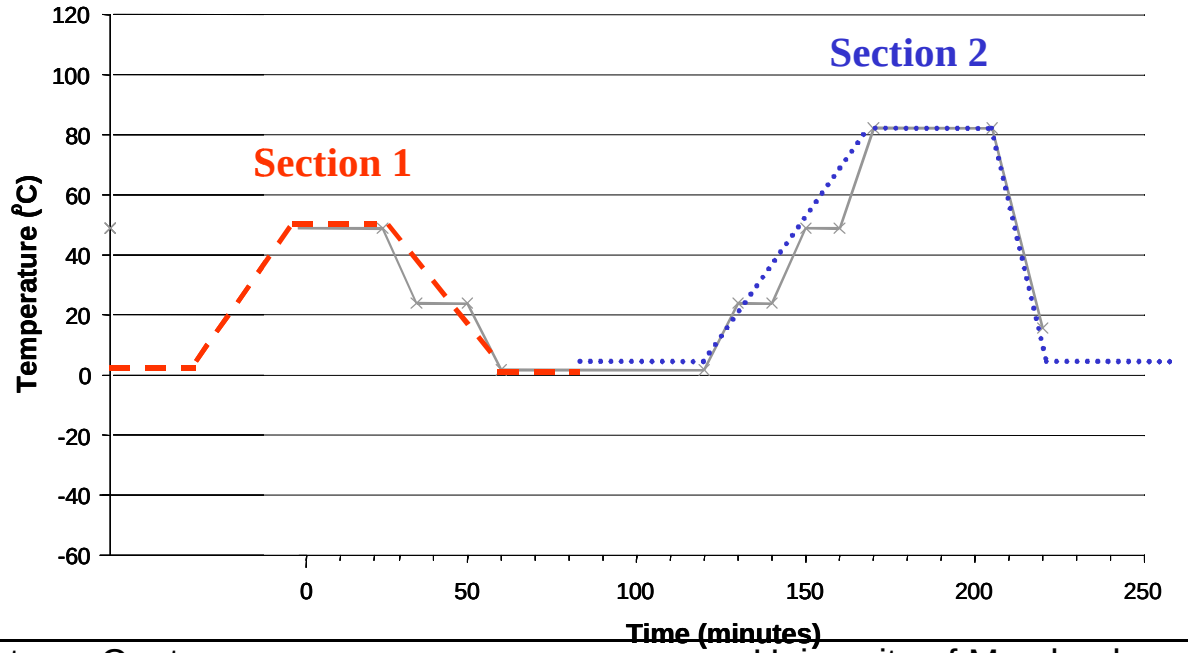
Life Cycle Loading Characterization

The temperatures shown in Table 1 were taken as inputs to the thermal analysis. Section 1 and section 2 are combined to account for one cycle.

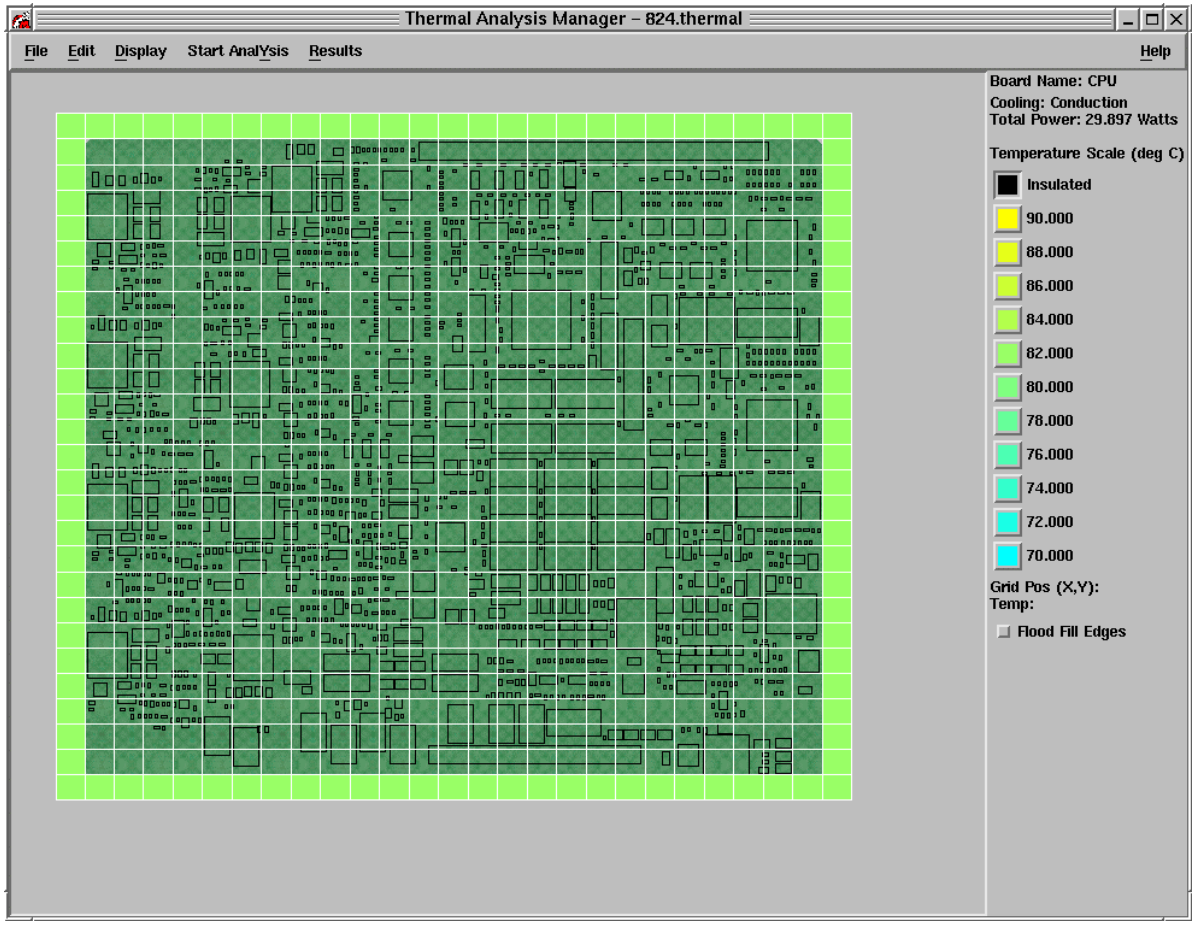
Use Category	Tmin (^{0}C)	Tmax (^{0}C)	Ramp time to Tmax/ to Tmin	Dwell at Tmax /Tmin	Time of Cycles	Total time
Section 1	9.5	49	35 min/ 35 min	25 min /30 min	175 min	365 days/ 10 year
Section 2	12.5	82	50 min/ 15 min	35 min /30 min	160 min	365 days/ 10 year

Table 1. Sections of **one** thermal cycle

AS900 nominal temperature profile for one cycle



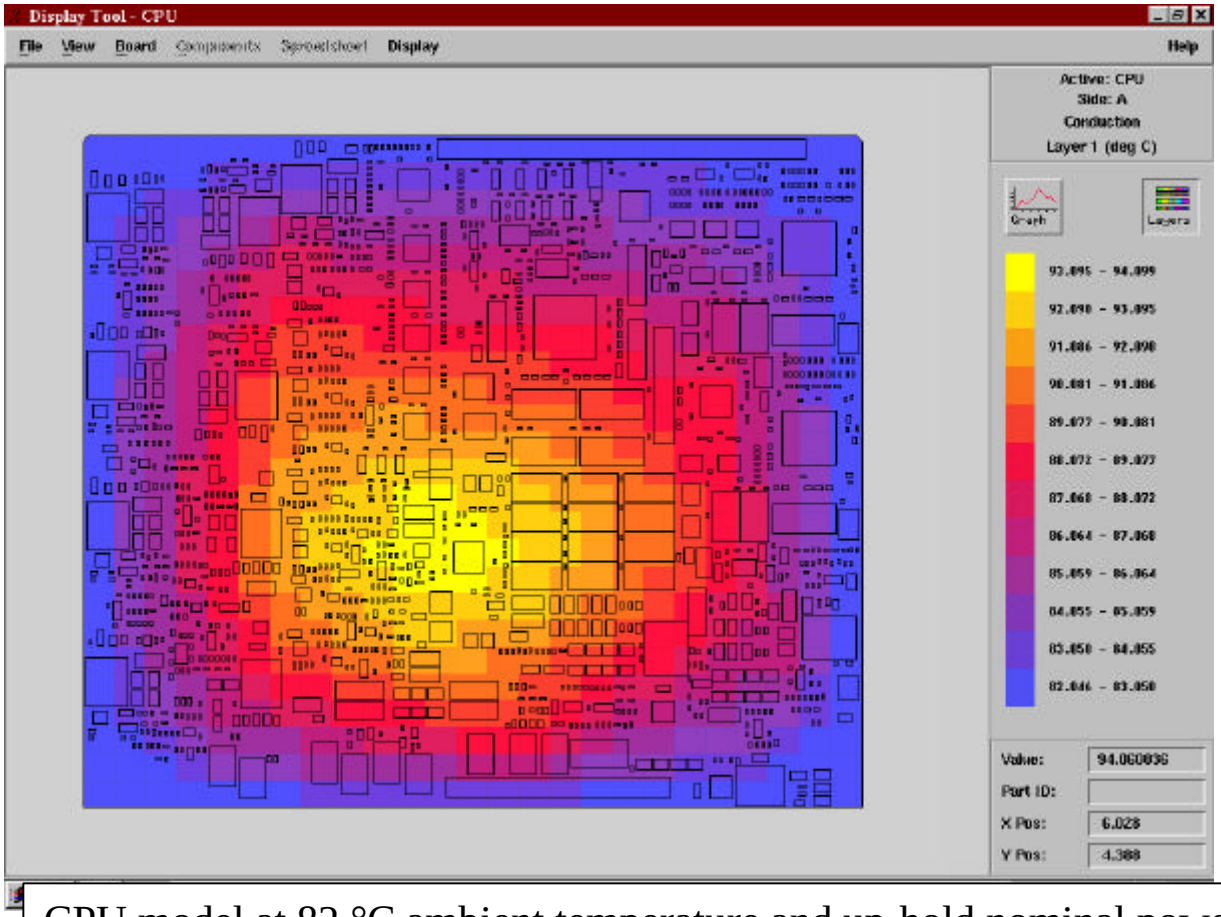
Load Transformation: Thermal Assessment



Thermal analysis results with an aluminum heat sink in the backside. The thermal analysis was simulated with pure conduction with no heat loss from the top and bottom surfaces.

Thermal Model	Total Power
CPU board	29.9
I/O board	8.7
EMI board	0.6

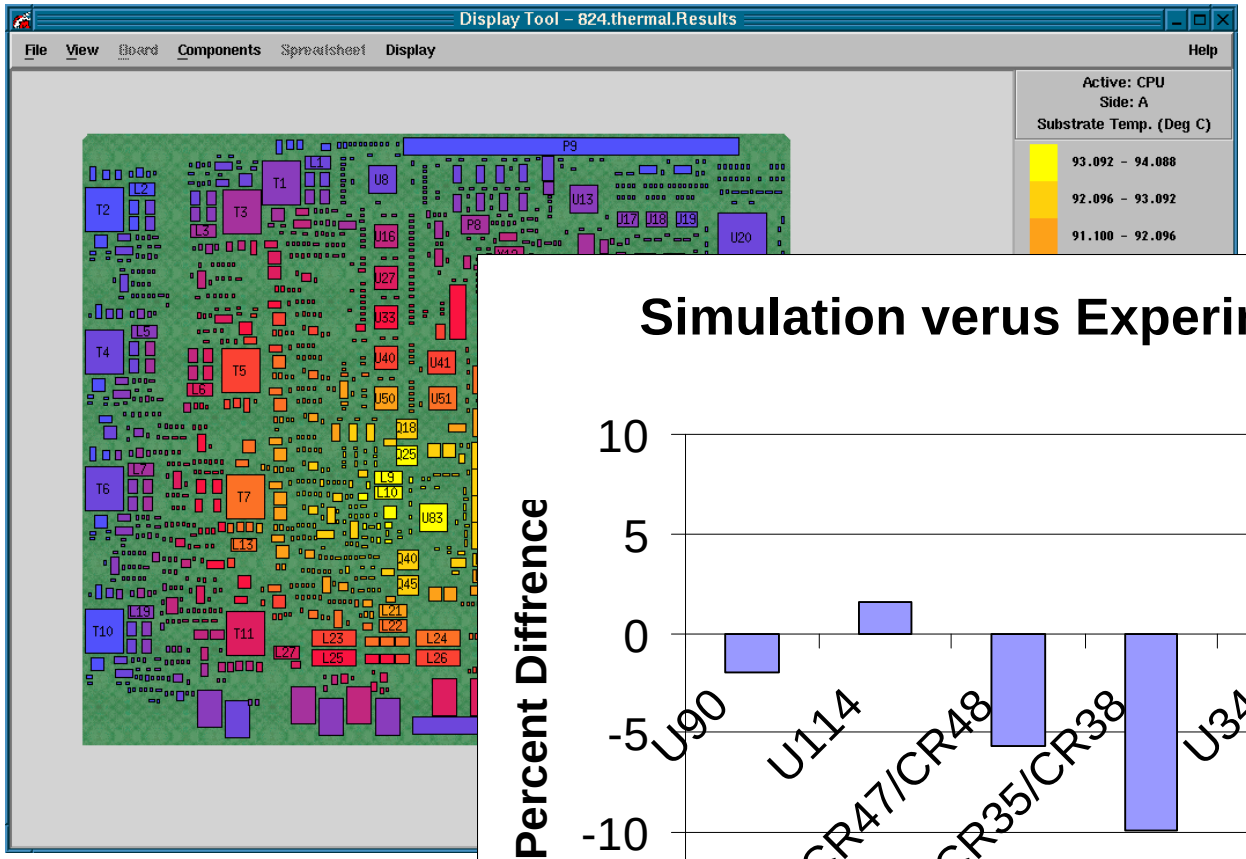
Load Transformation: Thermal Analysis Results

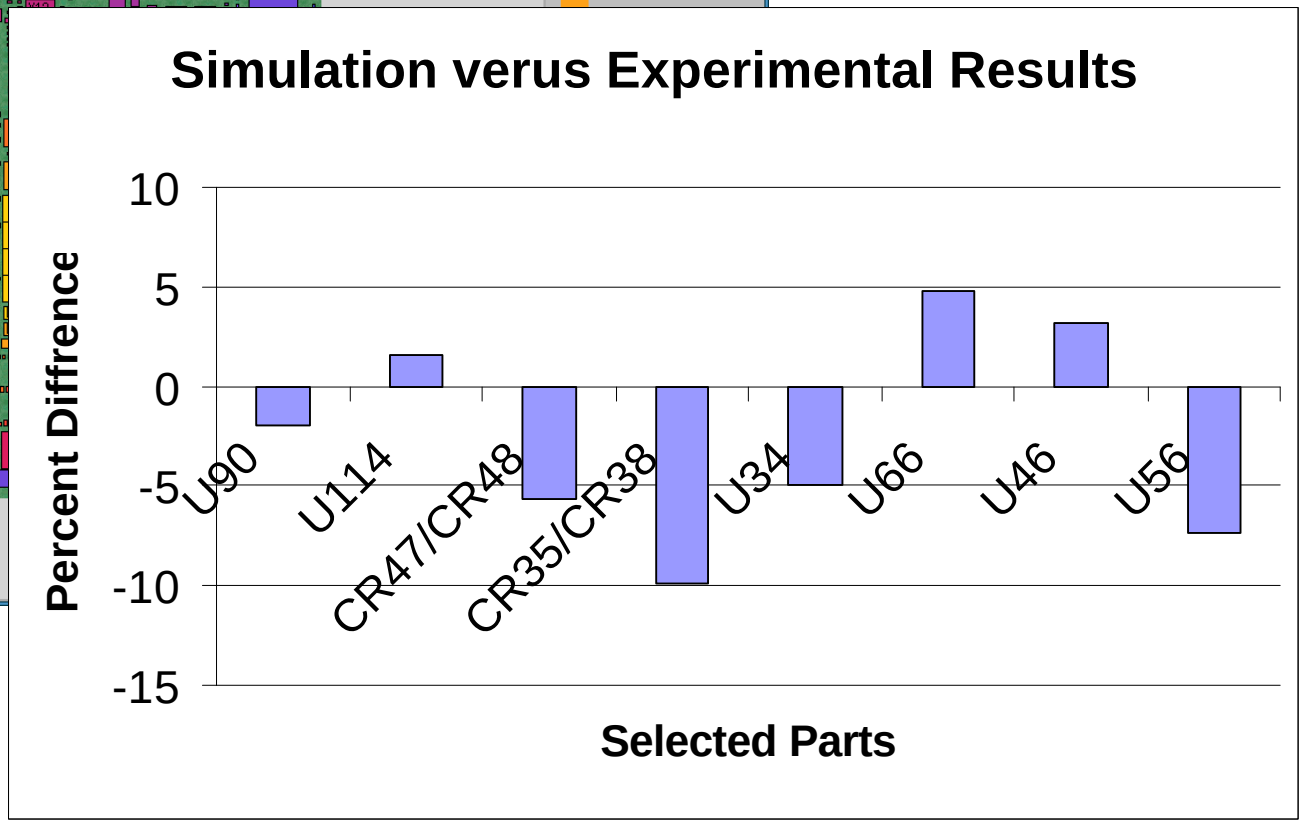


CPU model at 82 °C ambient temperature and up-hold nominal power

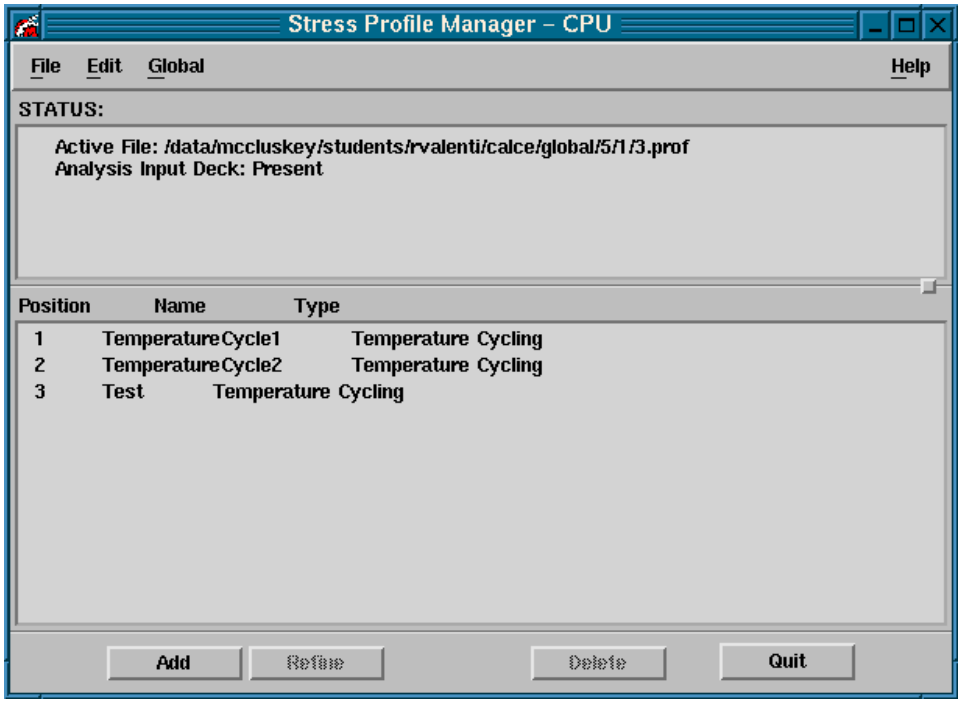
Thermal Model	Max Temp. (° C)
CPU board	94.0
I/O board	84.5
EMI board	82.1

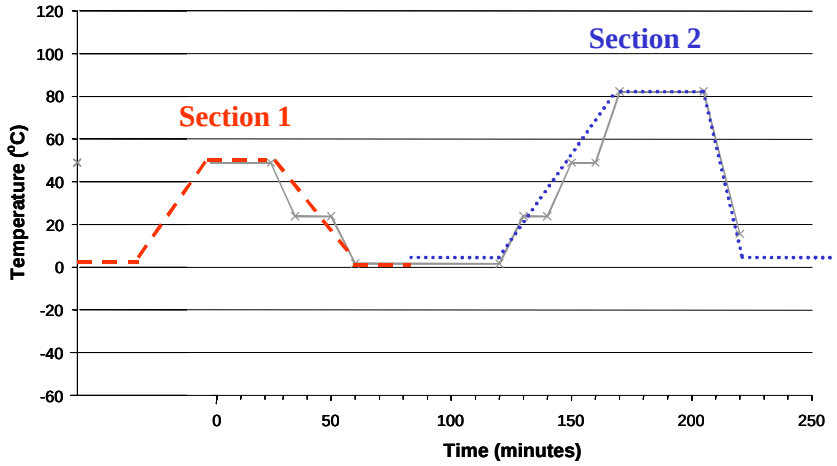
Comparison with Experimental Result

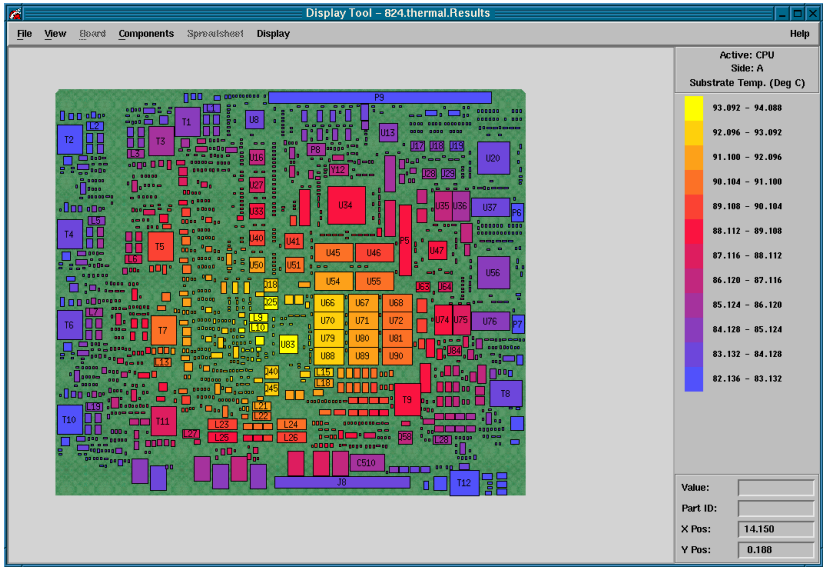




Defining the Life Cycle Stress Profile

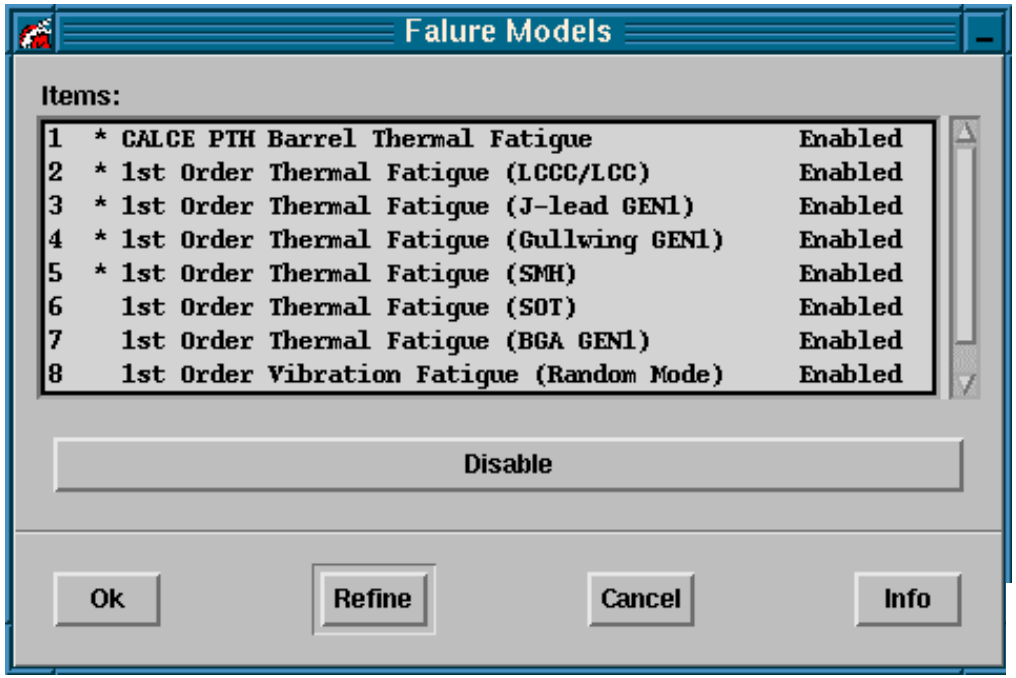




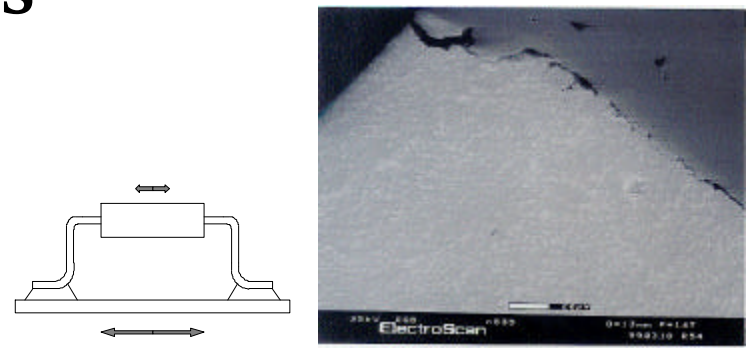


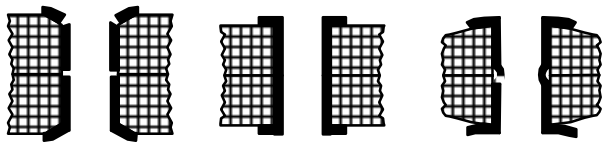
Stress profile was created using results of the thermal analysis runs considering the electronics be operational full time.

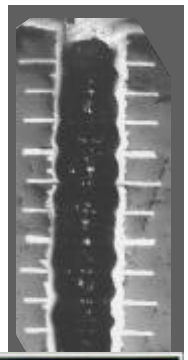
Failure Risk Assessment: Selecting Failure Models and Sites

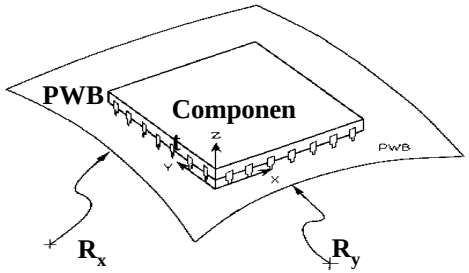


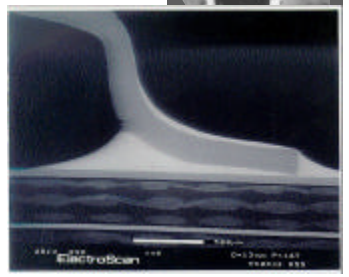
Failure Model Selection











Once a Life Cycle Stress Profile Database has been selected and the analysis mode and related information defined, the software will automatically screen the data to determine the set of applicable failure models. At this point, you can then review available failure sites.

Handling Multiple Environments for the Same Failure Site

Damage is defined as the percent of life removed from a functional structure. If we assume that data is accumulated in a linear fashion, then we can define a damage index as

$$D=\frac{n}{N}$$

where n is the applied time and N is the survivable time. Failure is defined if $n \geq N$ or $D \geq 1$.

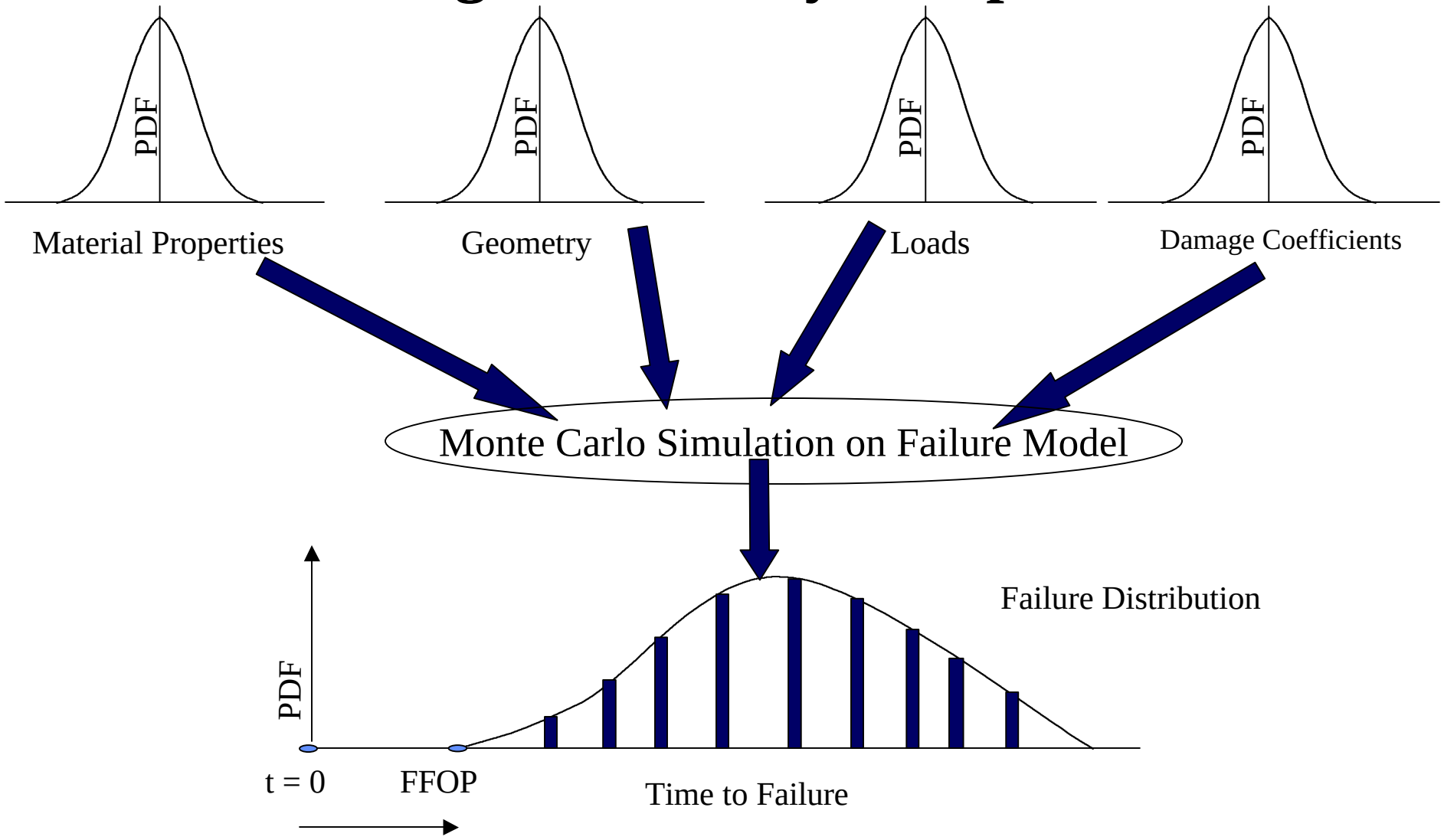
For multiple environments and the same failure site and mechanism. We can define the total damage as the sum of the damage indices for the individual environments or

$$D_{total}=\sum_{i} D_i$$

Failure is assumed to occur when $D_{total} \geq 1$

Caveat: The assumption of linear may not be valid for different failure mechanisms. One needs to understand the physical failure phenomenon to accurately determine the effect of multiple environmental factors.

Handling Uncertainty in Input Data



Failure Risk Assessment - Results

Results are presented through both tabular and color coded graphical displays. More detailed information is available for each failure site.

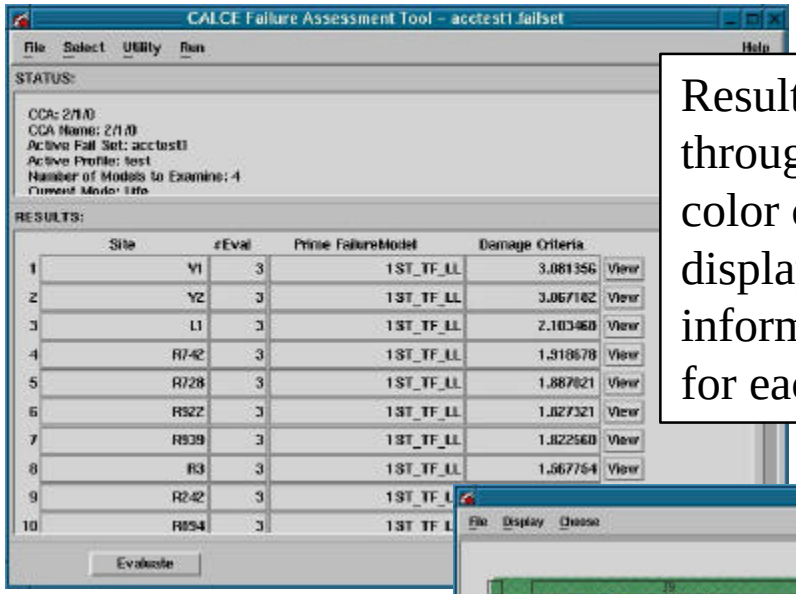
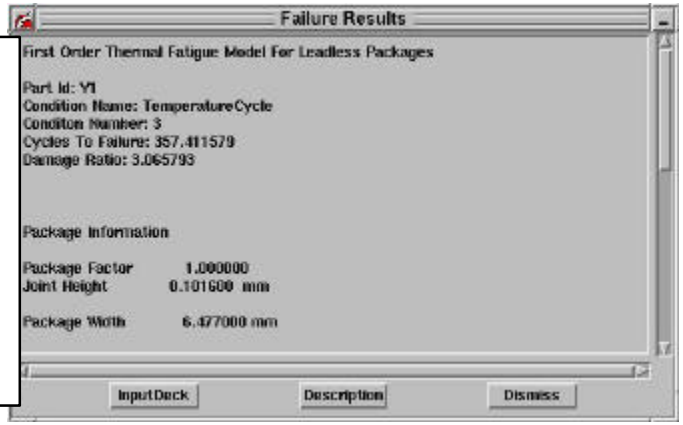
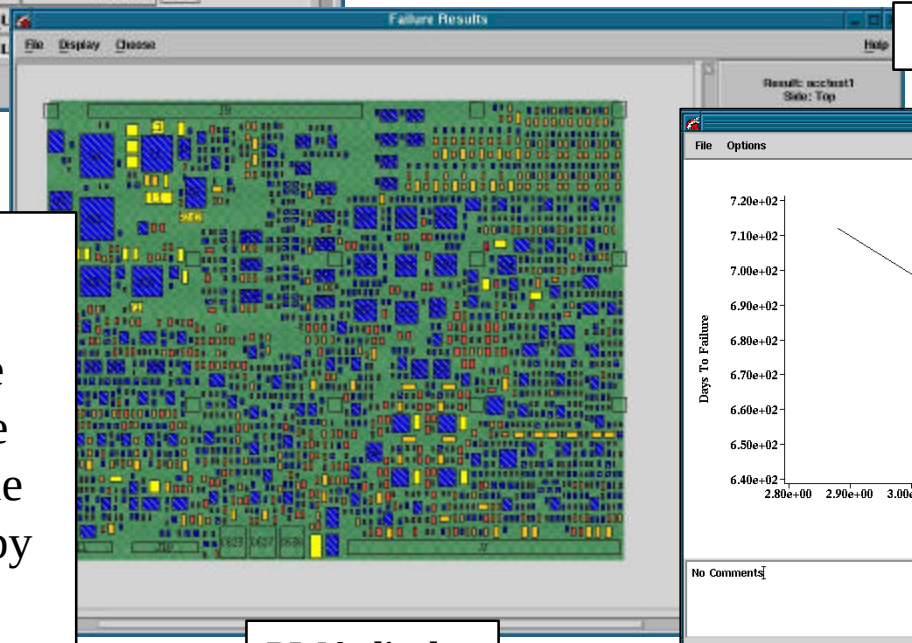


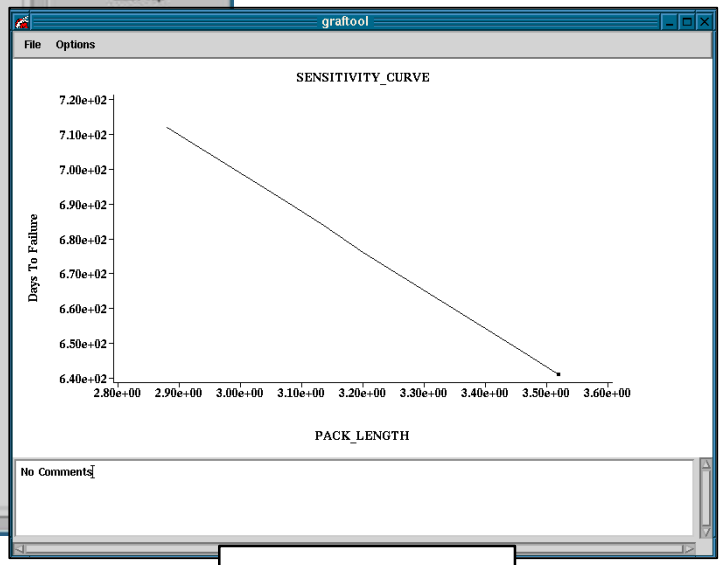
Table Display



Site Text Report



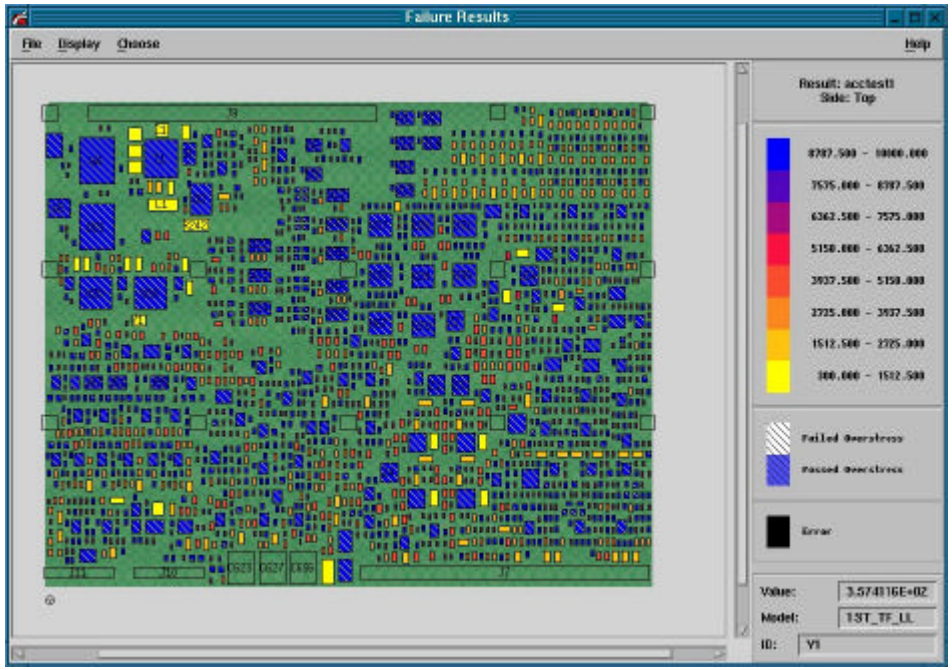
PWA display



Sensitivity Plots

Once the Life Profile and Failure Models and Sites have been selected, save the analysis problem to file and start the analysis by selecting ***Evaluate*** button.

Failure Risk Assessment - Results



Analysis indicates several design weaknesses: In particular

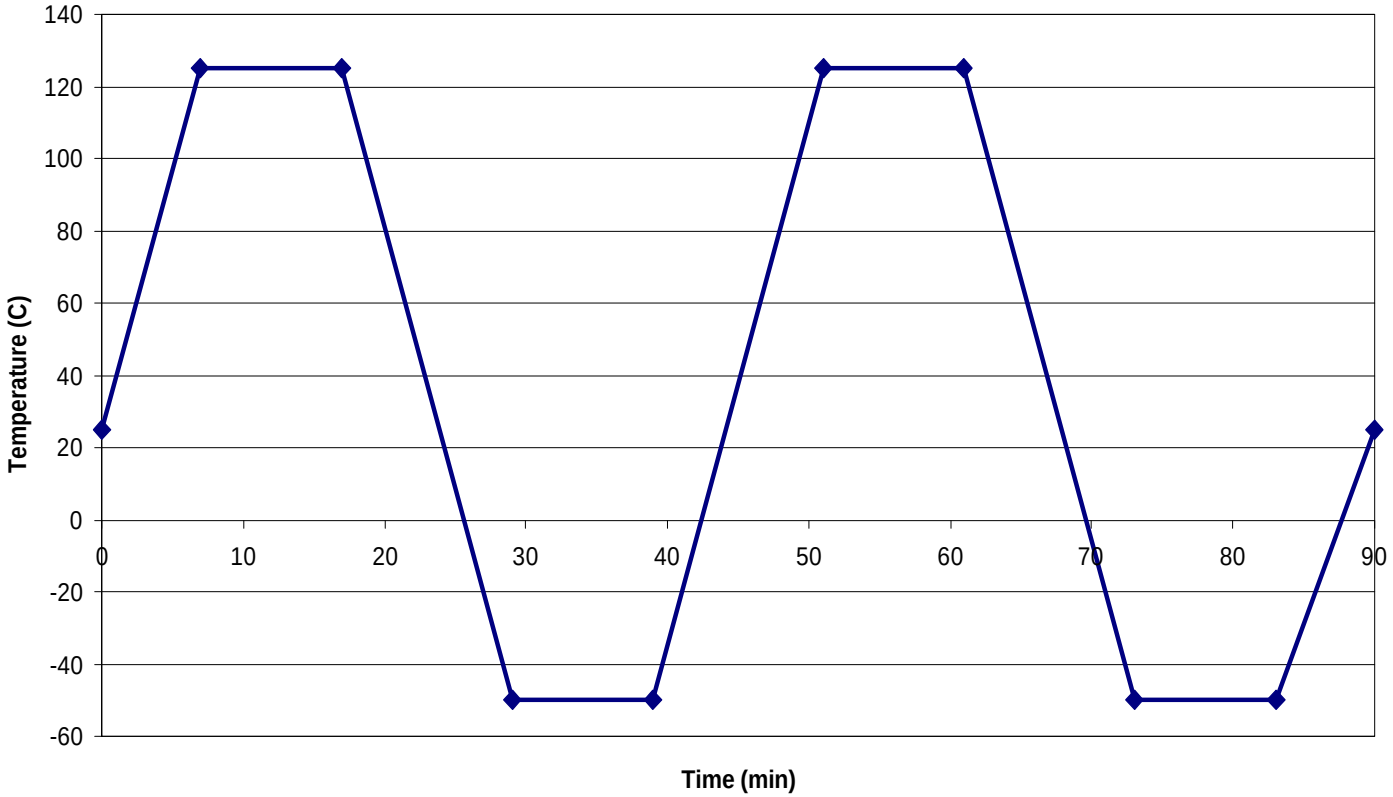
Clock Oscillator
1206 Chip Resistors
Transistor (SOT23).

Assessment indicates that these parts will not survive the design requirement.

Review and Verification: Physical Test

Temperature Cycle

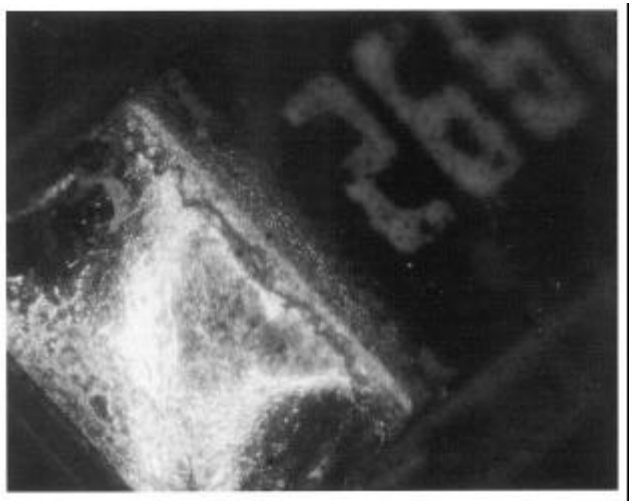
- -50 °C to 125 °C Temp limits
- 10 min. Dwell time
- 15 °C/min ramp rate
- ~45 cycles per day



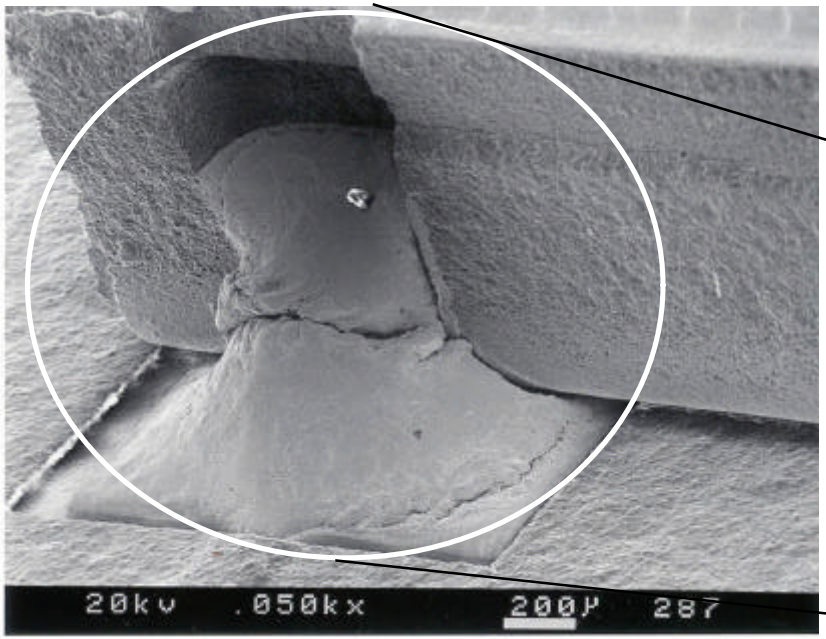
Board was inspected every 100 cycles until visible failure was noticed under magnification. Subsequent inspection was every 50 cycles.

Analysis of Failed Test Specimens

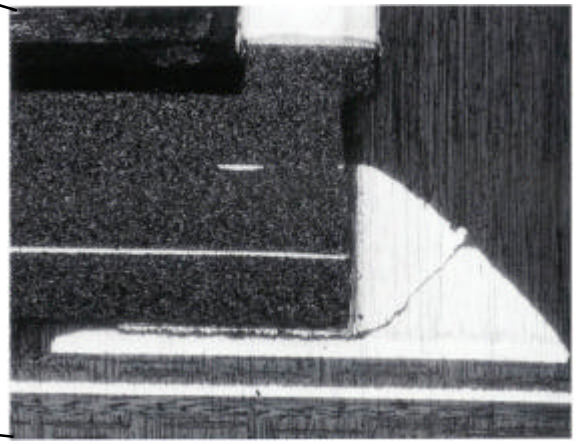
Accelerated test confirmed these weaknesses. Visible cracking of solder joints was observed at 300 cycles.



Fatigue Failure of 1206 Chip Resistor



Fatigue Failure of Clock Oscillator

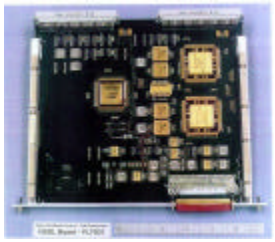


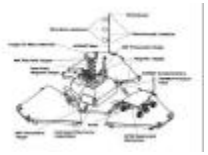
Cross-Section of Clock Oscillator Joint

Other demonstrations of virtual qualification

NASA-JPL

- Assessed four circuit cards assemblies (CCAs).
- Matched thermal analysis results.
- Confirmed robustness of design





JSTARS Ground Station

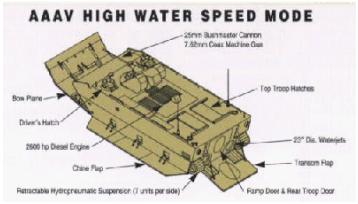
- Compared commercial and ruggedized designs
- Recommended commercial processor circuit card
- Estimated saving $1.2M

Tri-Service Radio

- Assessed three production CCAs
- Determined design would not meet life objective.
- Design change resulting in $25M

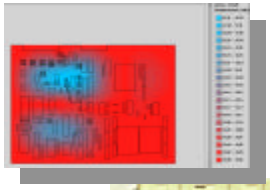
AAAV

- Assessed two of CCAs
- Provided test plan



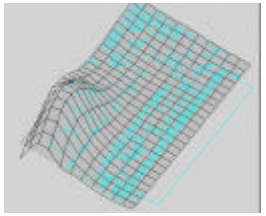
Bradley Fire Support Vehicle

- Assessed 15 CCAs
- Identified potential problems
- Confirmed vibration simulation results through test.



Automotive

- Assessed and tested CCA
- 83% reduction in design issues
- 10% reduction in time to market



Life Cycle PoF Analysis Provides Considerable ROI

Summary

• Reliability of product can be improved dramatically by conducting virtual qualification prior to building hardware.

• Automated software can be used to facilitate assessment process.

• Damage and stress models are effective for identifying intrinsic design deficiencies and for providing a relationship between test and field failures.

• Physical testing should be used to verification that simulation adequately captured the anticipated failures sites.